Abstract

An electronic circuit comprises a plurality of input/output (I/O) nodes for connecting the electronic circuit to a further electronic circuit via interconnects. A main unit implements a normal mode function of the electronic circuit. A test unit tests the interconnects. The electronic circuit has a normal mode in which the I/O nodes are logically connected to the main unit and a test mode in which the I/O nodes are logically connected to the test unit. In the test mode the test unit is operable as a low complexity memory via the I/O nodes.